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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,089	HIRAIDE ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2004 and 19 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendments dated 7/28/04 and 8/19/04. Claims 1-3, 6, 9-14, 20, and 29-31 have been amended.

Claims 7, 8, 32 and 33 have been cancelled.

Claims 1-6 and 9-31 are pending in this office action.

Response to Amendment

1. In view of the applicant's substitute Abstract, the examiner has withdrawn the objection to said Abstract.

2. In view of the applicant's replacement to the Specification at page 31, line 24, the examiner has not approved the change and maintains the objection. The examiner requests that the applicant correct the objection as follows: rewrite page 32 line 1 of the Specification from "Fig. 4 comprises..." to instead recite, "Fig. 23 comprises...".

3. In view of the applicant's replacement sheets for FIG.21 and FIG.22, the examiner withdraws the objection to said figures.

4. Applicant's arguments, see amendment, filed 7/28/04, with respect to the rejections of independent claims 1, 2, 3, 6, 29, 30 and 31 under 35 USC 102 and 103, have been fully considered and are persuasive. Therefore, the rejections to independent Claims 1, 2, 3, 6, 29, 30 and 31, as well as independent Claims 4, 6 and 9-28 have been withdrawn. However, upon further consideration, new grounds of rejection is made in view of the applicant's amendment to the said claims, and in view of the new reference art cited in below.

Claim Rejections - 35 USC § 103

5. Claims 1, 6, 9 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme".

As per Claims 1, 6, and 29:

Koenemann et al. teaches a testing method or circuit/apparatus for an integrated circuit column 3 lines 14-16) comprising: a pattern generator built in said integrated circuit to generate test patterns (column 5 lines 21-27); a plurality of shift registers configured with sequential circuit elements inside said integrated circuit (column 6 lines 60-66); and a pattern modifier (FIG.3) to modify a portion, to which a predetermined value is required to be set in order to detect a fault (column 5 lines 64-66 and column 5 lines 48-57), in said pseudo random patterns generated by said pattern generator (see FIG.3), and to input said modified pseudo random patterns to said shift registers (see FIG.4 20 and 19A-N) on a basis of said test patterns. But Koenemann et al. fails to teach an automatic test pattern generating unit to generate ATPG test patterns. But in an analogous art, Jas et al. teaches this feature in FIG.4, where the test patterns are stored in LUT, supplied by the Tester, which generates vectors for LUT by a well known ATPG method (see page 7 column 1, "doing ATPG for the remaining undetected faults"). The advantage for this approach is stated in the Abstract (reduces tester storage and bandwidth requirements while using less BIST overhead). One with

ordinary skill in the art at the time of the invention, motivated as suggested, would have found it to be obvious to include the ATPG practice of Jas et al. with the method of Koenemann et al.

As per Claim 9:

Koenemann et al. further teaches the testing apparatus according to claim 1, wherein said pattern modifier selects a suitable combination of one pseudo random pattern (FIG.4 PRPG output 1) and one ATPG pattern (FIG.4 weight storage RAM 1) from said pseudo random patterns generated by said pattern generator and said ATPG, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern (FIG.4 and FIG.3 circuit 20). And in view of the motivation previously stated, the claim is rejected.

6. Claims 11, 13, 15, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", and further in view of Farnsworth et al., U.S. Patent No. 6708305.

As per Claim 11:

Koenemann et al. and Jas et al. teach the limitations of Claim 1, but do not specifically teach modifying the PSRG pattern on the basis of said selected ATPG pattern. However, in an analogous art, Farnsworth et al. does teach this feature. Farnsworth et al. teaches modifying the PSRG pattern on the basis of said selected ATPG pattern (column 2 lines 33-67). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without requiring the high

bandwidth required by off-chip testers. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Farnsworth et al., would combine the art to produce a test system requiring low bandwidth deterministic type testing, and so the claim is rejected.

As per Claim 13:

Koenemann et al. and Jas et al. teach the limitations of Claim 1, but do not teach a characteristic information determining unit. However, in an analogous art, Farnsworth et al. does teach an apparatus further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns; wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit (see column 2 lines 33-67 and column 3 lines 1-17). And in view of the motivation previously stated, the claim is rejected.

As per Claim 15:

Farnsworth et al. further teaches the testing apparatus according to claim 13, and additionally wherein said characteristic information is a seed value to be set to said pattern generator (Farnsworth et al. column 4 lines 50-59). And, in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

As per Claim 17:

Farnsworth et al. further teaches the testing apparatus according to claim 13, wherein said pattern generator is configured as a linear feedback shift register (FIG.4 LFSR 10), and said characteristic information is a feedback position in said linear feedback shift register (FIG.4 input to LFSR 10 at 1).). And, in view of the previously recited motivation, the claim is rejected.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", and further in view of Rajski et al., U.S. Patent No. 6327687.

As per Claim 19:

Koenemann et al. and Jas et al. teach the testing apparatus according to claim 1, but fail to teach any limitations to a compression process. But in an analogous art, Rajski et al., does teach the feature; further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process; wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied (column 14 lines 45-67 and column 15 lines 1-8). And column 4 lines 25-33 explains that an advantage needed in the art is the ability to seed an LFSR quickly in order to better utilize tester time. And one with ordinary skill in the art at the time of the

invention, motivated by the aforementioned advantage, would have found it obvious to combine the references to speed up testing, and so the claim is rejected.

8. Claims 21, 23, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", in view of Rajski et al., U.S. Patent No. 6327687, and further in view of Rajski et al., U.S. Patent No. 5991909.

As per Claim 21:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 65-68). And in view of the motivation cited previously, the claim is rejected.

As per Claims 23:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 21, the testing apparatus according to claim 21, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected. .

As per Claim 25:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 19, the testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 30-67 and column 15 lines 1-8). And in view of the motivation cited previously, the claim is rejected.

As per Claim 27:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 25, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected.

9. Claims 2, 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnhart et al., "OPMISR: The Foundation for Compressed ATPG Vectors". As per Claims 2 and 30:

Barnhart et al. teaches a testing circuit/apparatus for an integrated circuit (page 748, column 1 Introduction) comprising: a plurality of shift registers to which test patterns are inputted (FIG.4 scan chains), configured with sequential circuit elements inside said integrated circuit (FIG.4 scan chains); a mask (FIG.2 mask) to convert an indeterminate value in outputs from said shift registers into a state value of '0" or "1" to mask said indeterminate value (page 751 column 2 2nd paragraph); and an output verifier (FIG.2 MISR) to verify output results in which said indeterminate value is masked by said mask (see FIG.2), said output results not containing said indeterminate value (page 751 column 2 2nd paragraph). Though the reference does not specifically state that the mask changes the input to the MISR to a "1" or a "0", one with ordinary skill in the art at the time of the invention would have recognized that, in view of the circuit design of the reference art, the inputs to the MISR in Figure 2 on page 751 (from the mask) must either be a "1" or a "0", and nothing else. Therefore, the examiner, being one of ordinary skill, and since the applicant has not further limited the mask operation, serves notice to the applicant that the claim is rejected as being obvious in respect to the values "1" and "0" of the claim, and so the claims are rejected.

As per Claim 4:

Barnhart et al. further teaches the testing apparatus according to claim 2, wherein said output verifier includes a compressing means for compressing said masked output results (Page 751 FIG.2 MISR). And in view of the motivation previously stated, the claim is rejected.

10. Claims 3, 5, 10 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", and further in view of Barnhart et al., "OPMISR: The Foundation for Compressed ATPG Vectors".

As per Claims 3 and 31:

The subject claims are a combination of Claims 1 and 2 above, and in view of the rejections on the said Claims 1 and 2, and in view of the motivations cited, the claims are rejected.

As per Claim 5:

Koenemann et al. further teaches the testing apparatus according to claim 3, wherein said output verifier includes a compressing means for compressing said masked output results (FIG.4 18 MISR). And in view of the motivation previously stated, the claim is rejected.

As per Claim 10:

Koenemann et al. further teaches the testing apparatus according to claim 3, wherein said pattern modifier selects a suitable combination of one pseudo random pattern (FIG.4 PRPG output 1) and one ATPG pattern (FIG.4 weight storage RAM 1) from said pseudo random patterns generated by said pattern generator and said ATPG, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern (FIG.4 and FIG.3 circuit 20). And in view of the motivation previously stated, the claim is rejected.

11. Claims 12, 14, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", and further in view of Barnhart et al., "OPMISR: The Foundation for Compressed ATPG Vectors".

As per Claim 12:

Koenemann et al. and Jas et al.and Barnhart et al. teach the limitations of Claim 3, but do not specifically teach modifying the PSRG pattern on the basis of said selected ATPG pattern. However, in an analogous art, Farnsworth et al. does teach this feature. Farnsworth et al. teaches modifying the PSRG pattern on the basis of said selected ATPG pattern (column 2 lines 33-67). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without requiring the high bandwidth required by off-chip testers. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Farnsworth et al., would combine the art, and so the claim is rejected.

As per Claim 14:

Koenemann et al. and Jas et al. and Barnhart et al. teach the limitations of Claim 3, but do not teach a characteristic information determining unit. However, in an analogous art, Farnsworth et al. does teach an apparatus further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator with which said pattern

generator can generate pseudo random patterns analogous to said ATPG patterns; wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit (see column 2 lines 33-67 and column 3 lines 1-17). And in view of the motivation previously stated, the claim is rejected.

As per Claim 16:

Farnsworth et al. further teaches the testing apparatus according to claim 14, and additionally wherein said characteristic information is a seed value to be set to said pattern generator (Farnsworth et al. column 4 lines 50-59). And, in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

As per Claim 18:

Farnsworth et al. further teaches the testing apparatus according to claim 14, wherein said pattern generator is configured as a linear feedback shift register (FIG.4 LFSR 10), and said characteristic information is a feedback position in said linear feedback shift register (FIG.4 input to LFSR 10 at 1).). And, in view of the previously recited motivation, the claim is rejected.

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", in view of Barnhart et al., "OPMISR: The Foundation for Compressed ATPG Vectors", and further in view of Rajski et al., U.S. Patent No. 6327687. Koenemann et al. and Jas et al. and Barnhart et al. teach the testing apparatus according to claim 3, but fail to teach

any limitations to a compression process. But in an analogous art, Rajski et al., does teach the feature; further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process; wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied (column 14 lines 45-67 and column 15 lines 1-8). And column 4 lines 25-33 explains that an advantage needed in the art is the ability to seed an LFSR quickly in order to better utilize tester time. And one with ordinary skill in the art at the time of the invention, motivated by the aforementioned advantage, would have found it obvious to combine the references to speed up testing, and so the claim is rejected.

13. Claims 22, 24, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenemann et al., U.S. Patent No. 5612963, in view of Jas et al., "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme", in view of Barnhart et al., "OPMISR: The Foundation for Compressed ATPG Vectors", in view of Rajski et al., U.S. Patent No. 6327687, and further in view of Rajski et al., U.S. Patent No. 5991909.

As per Claim 22:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one

ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 65-68). And in view of the motivation cited previously, the claim is rejected.

As per Claims 24:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 21, the testing apparatus according to claim 21, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected. .

As per Claim 26:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 19, the testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value (Rajski et al.

6327687 column 14 lines 30-67 and column 15 lines 1-8). And in view of the motivation cited previously, the claim is rejected.

As per Claim 28:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 25, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
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